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Vapor Deposition of Copper-Manganese Interconnects

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Abstract—**Chemical vapor deposition (CVD) of copper and manganese can produce interconnects scaled down to below 10 nm, while enhancing their conductivity and lifetime. CVD using similar super-conformal processes can enable very narrow through-silicon-vias, as well as tiny and robust flexible wires between chips. Silica insulating layers can be made by a super-conformal and rapid atomic layer deposition (ALD) process.**

Keywords— interconnects; through silicon vias; chemical vapor deposition; copper; manganese; diffusion barrier; void-free filling

I. LIMITATIONS OF CURRENT INTERCONNECT TECHNOLOGIES

The lower levels of copper interconnect technology within a chip faces many challenges as linewidths are being scaled down to 10 nm or below. Line resistances increase rapidly because the electron mean free path becomes limited by the linewidth. Conventional tantalum-based barriers exacerbate this effect by reducing the effective width remaining for copper, while contributing little to the overall conductivity of the line. Line resistance is also raised by the diffuse electron scattering at the copper-tantalum interface. Etching processes produce line-edge roughness that reduces reliability because tantalum-based barriers become too thin where they are shadowed by overhanging roughness.

Interconnects between stacked chips also cause bottle-necks in communication because they are usually routed around the edges of the chip. Shorter and faster communication between chips could be obtained by passing signals through the chip, but many challenges have hindered the adoption of through-silicon-vias (TSVs). Large-diameter holes have been required because of the limited step coverage of conventional tantalum-based barriers and copper seed layers. The large footprint of these holes renders too high a portion of the chips unusable for devices. Low throughput of copper plating, due to the high resistance of the non-uniform PVD copper seed layers, renders this process uneconomical.

Communicating between separated chips in flexible wearable devices could be enabled by robust tiny wiring between different types. For example, separate sensors could be attached to a central communications chip, and combined with a solar cell to power them. More robust and economical methods for flexible connection of signals and power between separate chips would enable integration of these separate components into powerful systems.

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All of these problems can be solved by using appropriate vapor deposition methods to make these interconnects.

II. NARROW INTERCONEECTIONS WITHIN CHIPS

The following process steps are proposed to form very narrow, low resistance and robust copper interconnects at the lowest levels within chips [1]:

- After etching of trenches and vias, conformal CVD of manganese nitride lines the walls and bottoms of trenches and vias;
- Diffusion of manganese to form a barrier selectively on silica insulators but not on copper
- CVD of a sub-monolayer of iodine onto the surface of the manganese nitride
- CVD of super-conformal, bottom-up void-free fill by copper-manganese alloy catalyzed by the iodine, as shown in Fig. 1.
- CMP removes the overburden of copper-manganese alloy.
- PECVD of silicon carbonitride covers the planarized surface
- The manganese diffuses out of solution in the copper to the interfaces between the copper and the insulators, including the top SiCN, leaving pure, low-resistivity copper inside the interconnects.
- Manganese arriving by diffusion up to the copper/insulator interfaces increases further the bond strength between the copper and the insulator at those interfaces.

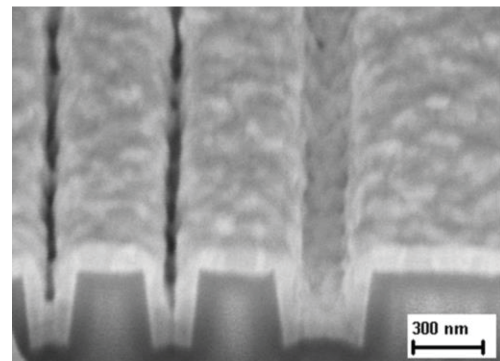

Fig. 1. Bottom-up growth by iodine-catalyzed CVD of copper-manganese alloy.

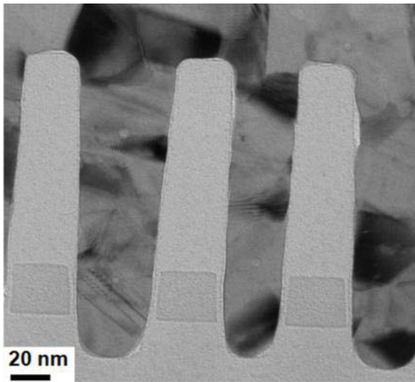

Fig. 2. Void-free filling of narrow trenches by iodine-catalyzed CVD of copper-manganese alloy.

The result of these steps is to make void-free, pure, low-resistance copper wires encased inside strongly adherent diffusion barriers inside trenches even narrower than 8 nm.

III. THROUGH-SILICON-VIAS BETWEEN STACKED CHIPS

Interconnects between chips also cause bottle-necks in communication because they are usually routed around the edges of the chip. Shorter and faster communication between chips could be obtained by passing signals through the chip, but many challenges have hindered the adoption of through-silicon-vias (TSVs). Large-diameter holes have been required because of the limited step coverage of conventional tantalum-based barriers and copper seed layers. The large footprint of these holes renders too high a portion of the chips unusable for devices. Low throughput of copper plating, due to the high resistance of the non-uniform PVD copper seed layers, renders this process uneconomical.

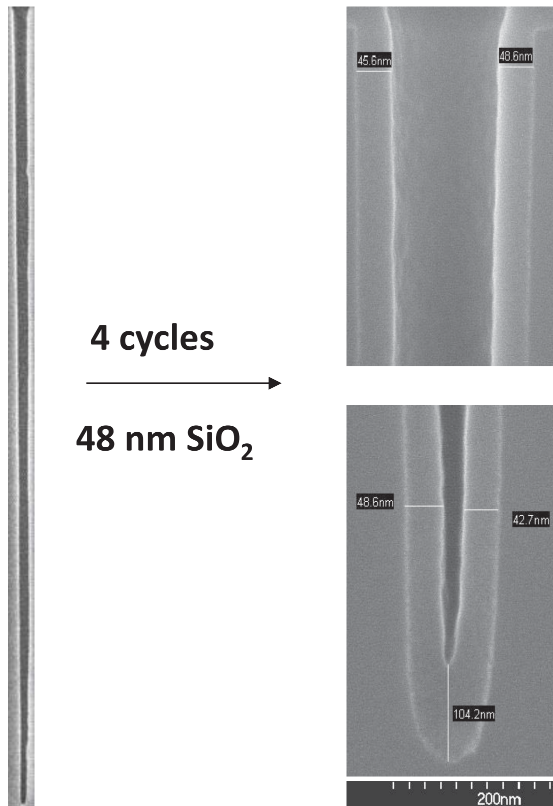

Fig. 3. ALD of alumina-doped silica as an insulator for TSVs.

The first step in making narrower TSVs is to deposit a highly conformal insulation layer between the silicon and the copper conductor that will then be deposited through it. Atomic layer deposition (ALD) of a silica-based insulator can be achieved by an unusually rapid version of ALD [2]. A single ALD cycle taking just a few seconds can deposit up to 20 nm of silica uniformly inside a TSV hole with length/width ratio even higher than 100:1, as shown in Fig. 3.

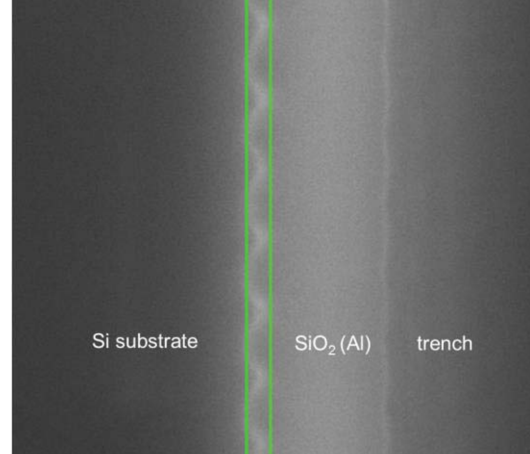

Fig. 4. ALD of super-conformal aluminum-doped silica with a smooth top surface grown on scalloped etched side-walls.

This ALD process is actually super-conformal, in that deposition on a scalloped sidewall left by the Bosch process fills in the scallops. The surface of the silica becomes flat, as shown in Fig. 4, because the growth rate in the valleys of the scallops is higher than on the peaks. This bottom-up growth is a consequence of the unusual ALD mechanism [2].

After the deposition of alumina-doped silica, copper-manganese alloy is deposited by the same steps outlined above for the narrow interconnects within chips. An example of a TSV layer is shown in Fig. 5 [3]. The manganese diffuses rapidly through the Cu-Mn alloy to the insulator surface during or after deposition, where it provides a barrier to keep the copper from diffusing into the silica insulator or the surrounding silicon. The manganese at that interface also increases the adhesion of the copper to the insulator surface, ensuring stability of the TSV structure.

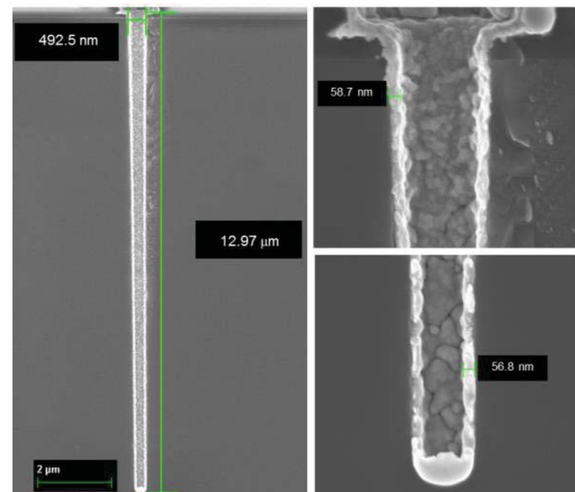

Fig. 5. CVD copper layer inside a narrow, high-aspect ratio hole

For signal transmission between chips, the resulting hollow cylinder of pure copper may provide a sufficiently low electrical resistance. In that case, the interior of the copper cylinder may be filled with ALD silica [2] for improving the mechanical stability. Thermal expansion mismatch between the TSVs and the surrounding silicon could damage the silicon. Such damage to the silicon could be minimized by choosing the correct ratio of more rapidly expanding Cu to the more slowly expanding SiO_2.

For power transmission through TSVs, it may be necessary to fill the TSVs with copper, to provide a higher conductivity than available through a hollow cylinder of copper. This copper fill could be done more economically by electroplating, using the CVD copper as a seed layer. An example of TSVs filled with copper by electroplating is shown in Fig. 6.

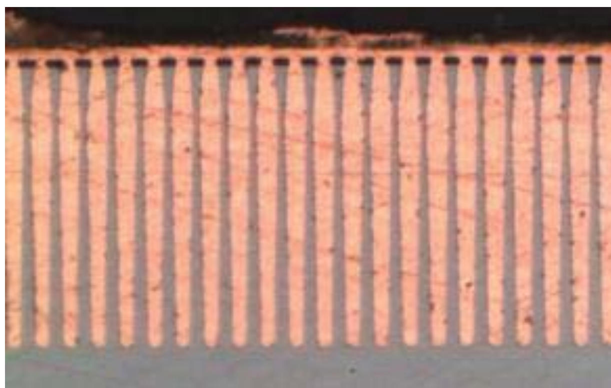

Fig. 6. TSVs filled with copper by electroplating onto a CVD Cu-Mn seed layer.

PVD seed layers are restricted to holes with aspect ratios less than about 20:1 because they become too thin near the bottoms of the holes. Another problem with PVD seed layers is that they require excessively long plating times because of their high, non-uniform resistance. This CVD seed layer has a much shorter plating time because of its uniformly low resistance along its whole length.

IV. Tiny, Robust Flexible Wires Between Chips

Wearable electronics can benefit from flexible, but robust interconnections between heterogeneous chips. For example, one might be a solar cell to provide power, another to provide computing power and data storage, another to provide RF communication and another to sense properties of a person or their environment.

The required high strength, flexibility and electrical conductivity could be combined in nanowires built on high-strength, thermally-stable polymers, such as polyaramids (Kevlar, Nomex or Zylon). As an example, CVD of copper-manganese alloy was carried out on Kevlar fibers at around 200 ^oC, as shown in Fig.7.

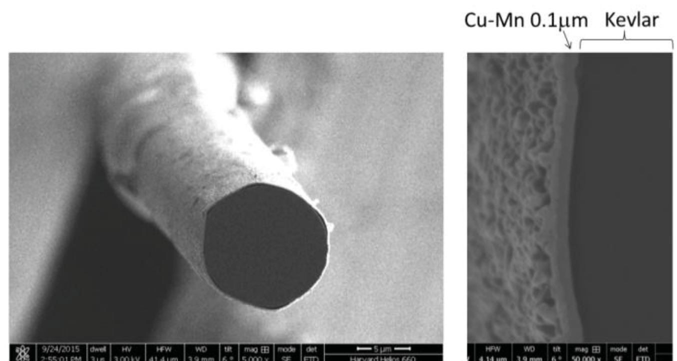

Fig. 7. SEM of a Kevlar fiber 11 μm in diameter coated with 0.1 μm CVD copper-manganese alloy. On the right, a closer view of the Cu-Mn coating.

The manganese provides strong adhesion to the oxygen and nitrogen atoms in these polymers. ALD of aluminum-doped silicon dioxide was then applied at a substrate temperature of about 250 ^oC to provide electrical insulation to the wires. This tiny wire can support more than a kilogram force without breaking. In a durability test in our laboratory, a wire was bent to a radius of 5 mm and then straightened more than half a million times without changing the electrical resistance of the wire. This kind of wire could provide durable, flexible interconnections between different kinds of chips

V. Conclusions

Vapor deposition has the potential to improve copper interconnect technology at all levels. The smallest copper wires on the lower levels of metallization can be made more conductive using super-conformal CVD of copper-manganese alloy. The manganese forms self-aligned barrier and adhesion layers. Through-silicon vias can be constructed in holes even narrower than anticipated by the roadmap. Flexible connections between chips can be fashioned by CVD of Cu-Mn and SiO_2 on high-strength polymer fibers.

Acknowledgments

Robert Mikkola carried out the electroplating shown in Fig. 6. Parts of this work were performed at the Harvard University Center for Nanoscale Systems.

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